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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,397	03/19/2004	Sun-Jay Chang	TSM03-0695	7350

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SLATER & MATSIL, L.L.P.
17950 PRESTON ROAD, SUITE 1000
DALLAS, TX 75252

EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,397	CHANG ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's Amendment and RCE filed May 12, 2006. Claims 1-20 are pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

1. Claims 1,4-12,15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jung et al (6,335,279) taken with Fulford (5,847,428) and Peng (6,004,851).

Re claim 1, Jung teaches (at Figs 3C-3M; col 6, line 15 through col 9) a method for forming a semiconductor device comprising at least the steps of: providing a substrate having a gate electrode 116 formed thereon (Figs 3D; col 6, lines 41-49); performing a first ion implant to form region 122a-122b wherein the gate electrode 116 acts as a mask (Fig 3E, col 6, lines 50-60); forming a first spacer 124 on the substrate adjacent to the gate electrode (Fig 3F, col 6, line 61 through col 7); forming an etch stop layer 126 on the substrate such that the etch stop layer 126 covers the first spacer 124 and the substrate (Fig 3G; col 7, lines 13-25); forming a sacrificial spacer 132 on the etch stop layer 126 on the substrate adjacent to the first spacer 124 (Fig 3I; col 7, lines 13-48); performing a second ion implant wherein the sacrificial spacer and the first spacer acts as a mask; and removing the sacrificial spacer 132 (Fig 3J, col 8, lines 1-8). Re claim 12, Jung teaches (at Figs 3C-3M; col 6, line 15 through col 9) a method for forming a semiconductor device comprising at least the steps of: providing a substrate having a gate electrode 116 and a shallow trench isolation (STI) 104 formed thereon (Figs 3D; col 6, lines 41-49; lines 8-15); forming a lightly doped drain 122a-122b in the substrate adjacent to the gate electrode 116 (Fig 3E, col 6, lines 50-60); forming a first spacer 124 on the substrate adjacent to the gate electrode (Fig 3F, col 6, line 61 through col 7); forming an etch stop layer 126 over the substrate 100, the first spacer 124, and over the STI 104 (Fig 3G; col 7, lines 13-25); forming a sacrificial spacer 132 on the etch stop layer 126 adjacent to the first spacer 124, the etch stop layer 126 preventing damage to the STI (Fig 3I, col 7, lines 13-48,44-48); performing a second ion implant wherein the sacrificial spacer and the first spacer acts as a mask; and removing the sacrificial spacer 132 (Fig 3J, col 8, lines 1-8). Re claim 4, wherein the etch stop layer 126 covers a shallow trench isolation 104 (Fig 3G; col 7, lines 13-25; and Fig 3D; col 6, lines 41-49;

lines 8-15). Re claim 6, wherein the first spacer comprises a silicon nitride (col 6, line 64 through col 7, line 25). Re claims 7,19, wherein the etch stop layer 126 is an oxide (col 7, lines 13-19). Re claims 8-9,16,18, wherein the sacrificial spacer 132/128 comprises a silicon nitride (Si3N4) (col 7, lines 19-55), and performing an anisotropic dry etch back (col 9, lines 15-20; col 7, lines 25-36; col 1, lines 45-54). Re claims 10,20, wherein the etch stop layer 126 is an oxide formed by chemical vapor deposition techniques (col 7, lines 15-19). Re claims 11,17, wherein removing the sacrificial layer 132 is performed by an etch process using a solution of phosphoric acid (col 8, lines 1-8).

Re claims 1 and 12, Jung already teaches removing the sacrificial spacer 132 to retain the etch stop layer and the first spacer having substantially the same shape as achieved in the step of forming a first spacer. Jung just lacks performing a third ion implant through the etch stop layer with the first spacer acts as a mask (claims 1 and 12). Re claims 5,15, performing a third ion implant before forming a second ion implant.

However, Fulford teaches (at Figs 13-15) after removing the sacrificial spacer 160, forming a doped region by performing a third ion implant 182 with the first spacer 136 as a mask, the third ion implant being performed through the etch stop layer 146 (as the CVD deposited etch stop layer 146 is an entire layer over the substrate, Fig 9; col 8, lines 42-66; and Figs 15,14; col 9, line 66 through col 10, line 67; Figs 9-14), after forming second ion implantation 170, wherein the first spacer is having substantially the same shape as achieved in the step of forming a first spacer. Re claim 5, Fulford also alternatively teaches (at Figs 8-12) performing a third ion implant 140 to form a doped region (Fig 8; col 8, lines 30-67) before forming a second ion implant 164 (Fig 12; col 9 lines 1-30). Peng also teaches (from Fig 2e to 2h) after removing the sacrificial spacer 22a (Fig 2e, col 4, lines 25-35), performing a third ion implant to form a doped region 25 with the first spacer 21b as a mask (Fig 2h; col 4, lines 39-49).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the semiconductor device of Jung, after removing the sacrificial spacer, by performing a third ion implant wherein the first spacer acts as a mask, as taught by Fulford and Peng, wherein the third ion implant is performed through the etch stop layer, as disclosed by Fulford. This is because of the desirability to form an enhanced lightly doped

region so as to reduce reverse junction leakage current and further suppress hot carrier effects, wherein the lightly doped region can be formed in the substrate by implanting ions into the substrate, either before or after the second ion implanting as an alternative way.

2. Claims 2-3,13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jung et al (6,335,279), Peng (6,004,851) and Fulford (5,847,428), as applied to claims 1,4-12,15-20 above, taken with Bu et al (6,812,073).

The references including Jung teach (at Figs 3C-3M; col 6, line 15 through col 9) a method for forming a semiconductor device, as applied to claims 1,4-12,15-20 above.

Jung already teaches etching to form the first spacer 124 (Figs 3F-3M), but lacks forming a dielectric liner acts as an etch stop (claims 2,13), wherein exposed portions of the dielectric liner are removed after forming the first spacer (claims 3,14).

However, Bu teaches (at Figs 1B-1C) forming the first spacer 30 and forming a dielectric liner 28 (Fig 1B) on the substrate, and etching a spacer layer to form the first spacer 30 wherein the dielectric liner 30 acts as an etch stop (col 4, lines 17-27; col 3, line 58 through col 4, lines 54).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the semiconductor device of Jung by further forming a dielectric liner on the substrate and acting an etch stop during etching to form the first spacer, as taught by Bu. This is because of the desirability to protect the underlying layers, and to prevent significant effect and damage to other layers during etching to form the first spacer.

Response to Amendment

3. Applicant's arguments with respect to pending claims 1-20 have been considered but they are not persuasive, and are moot in view of the new ground(s) of rejection.

** Jung already teaches forming the etch stop layer 126 over the substrate and the first spacer 124, wherein the first spacer is having substantially the same shape as achieved in the step of forming a first spacer. Fulford teaches (at Figs 13-15) after removing the sacrificial spacer 160, forming a doped region by performing a third ion implant 182 with the first spacer 136 as a mask, the third ion implant being performed through the etch stop layer 146 (as the CVD

deposited etch stop layer 146 is an entire layer over the substrate, Fig 9; col 8, lines 42-66; and Figs 15,14; col 9, line 66 through col 10, line 67; Figs 9-14), wherein the first spacer is having substantially the same shape as achieved in the step of forming a first spacer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the semiconductor device of Jung, after removing the sacrificial spacer, by performing a third ion implant wherein the first spacer acts as a mask, as taught by Fulford and Peng, wherein the third ion implant is performed through the etch stop layer, as disclosed by Fulford. This is because of the desirability to form an enhanced lightly doped region so as to reduce reverse junction leakage current and further suppress hot carrier effects, wherein the lightly doped region can be formed in the substrate by implanting ions into the substrate.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Oacs-18

Michael Trinh
Primary Examiner